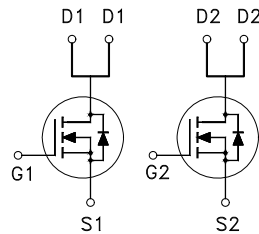


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	20V
R _{DS(on)} (MAX.)	14.8mΩ
I _D	7A



UIS 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±12	V
Continuous Drain Current	T _A = 25 °C	I _D	7	A
	T _A = 100 °C		5	
Pulsed Drain Current ¹		I _{DM}	28	
Avalanche Current		I _{AS}	10	mJ
Avalanche Energy	L = 0.1mH, I _D =10A, R _G =25Ω	E _{AS}	5	
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	2.5	
Power Dissipation	T _A = 25 °C	P _D	2	W
	T _A = 100 °C		0.8	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=10V, L=0.1mH, V_G=4.5V, I_L=7A, Rated V_{DSS}=20V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		25	°C / W
Junction-to-Ambient ³	R _{θJA}		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³62.5°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.4	0.8	1.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 12V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16V, V_{GS} = 0V$			1	μA
		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 4.5V$	7			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 4.5V, I_D = 7A$		13	14.8	m Ω
		$V_{GS} = 2.5V, I_D = 5A$		19	23	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 7A$		9		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 10V, f = 1MHz$		700		pF
Output Capacitance	C_{oss}			208		
Reverse Transfer Capacitance	C_{rss}			187		
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 10V, V_{GS} = 4.5V, I_D = 7A$		10		nC
Gate-Source Charge ^{1,2}	Q_{gs}			1.8		
Gate-Drain Charge ^{1,2}	Q_{gd}			3.7		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6\Omega$		15		nS
Rise Time ^{1,2}	t_r			20		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			30		
Fall Time ^{1,2}	t_f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I_S				2.3	A
Pulsed Current ³	I_{SM}				9.2	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.2	V

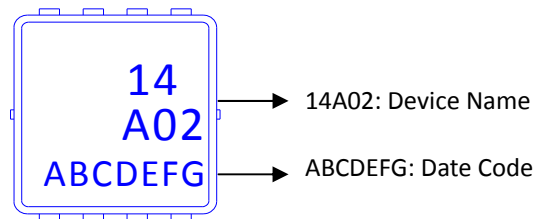
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

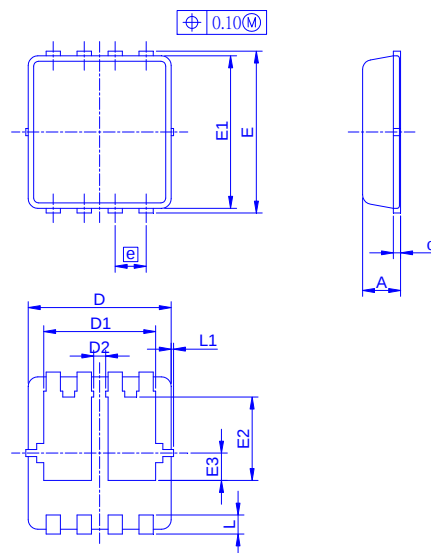
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB14N02BD for EDFN 3 x 3



Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	E3	e	L	L1	θ1
Min.	0.70	0	0.24	0.10	2.95	2.25		3.15	2.95	1.65			0.30	0	0°
Typ.	0.80		0.30	0.152	3.00	2.35	0.225	3.20	3.00	1.75	0.575	0.65	0.40		10°
Max.	0.90	0.05	0.35	0.25	3.05	2.45		3.25	3.05	1.85			0.50	0.10	12°

Recommended minimum pads

